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Modulating self-heating effects in FinFETs through doping engineering

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ABSTRACT

While FinFETs are widely adopted in advanced nodes for high-performance integration, their elevated power density induces pronounced self-heating effects that pose significant challenges to device reliability and performance, underscoring the importance of effective strategies for mitigating self-heating effects. By combining electro-thermal simulations based on the drift-diffusion model with phonon Monte Carlo (MC) simulations, this work elucidates the heat generation mechanisms in FinFETs and accordingly proposes a doping-engineering approach to mitigate self-heating effects. The results indicate a shift in the dominant heat generation mechanism with operating bias. While Joule heat is the primary heat generation mechanism under the saturation bias, the contribution from Thomson heat becomes significant under the typical CMOS operating bias, emerging as the dominant driver of heat generation non-uniformity due to its highly localized distribution in devices with reduced feature sizes. As a result, Thomson heat provides a pronounced contribution, approximately 16%, to the maximum device temperature rise. To address this issue, it has been found that reducing the doping concentration gradient in the device extension region can significantly reduce Thomson heat without decreasing the electrical performance, whereby the peak Thomson heat is reduced by 66% and the hotspot temperature rise is decreased by 13%. These findings provide insights into the self-heating behavior of FinFETs and suggest a potential approach for device-level thermal management.

Fin field-effect transistors (FinFETs) have become the dominant transistor architecture in modern IC manufacturing, enabling high-performance and low-power applications through superior electrostatic control.[1] However, their scaled dimensions and increased power densities give rise to pronounced self-heating effects,[2,3] which present a major challenge for performance[4,5] and reliability.[6,7] As a result, mitigating self-heating effects at the transistor level has become an important consideration in modern thermal management strategies.[8–10] Prior investigations have concentrated on lowering the thermal resistance within the device to facilitate more effective heat dissipation. Specifically, efforts have been devoted to modifying the thickness of shallow trench isolation layers,[3] and tailoring the thermal conductivity of oxide materials.[11,12] These strategies have effectively enhanced the predominantly one-dimensional heat transfer pathway from the channel region to the substrate, thereby markedly mitigating the temperature rise within the device.

However, within the transistor channel, the internal temperature rise is predominantly governed by three-dimensional heat spreading.[13] Moreover, as the characteristic dimensions of devices approach the nanometer scale, the presence of nanoscale heat sources further amplifies ballistic transport effects,[14] thereby exerting a pronounced influence on the heat spreading process.[15] As a result, the channel temperature distribution is governed by the spatial characteristics of heat generation, underscoring the necessity of modulating the heat profile to alleviate self-heating and enhance device performance. This strategy has already been implemented for gallium nitride (GaN) high-electron-mobility transistors (HEMTs).[16] However, in FinFETs, two aspects merit particular attention. On the one hand, due to their prevalent application in CMOS technology,[17] their operating condition is not constantly held at the highest current and voltage point, as is typically assumed in most thermal studies;[18] instead, their condition is continuously changing, and the current often peaks at half the saturation point.[19] On the other hand, their scaled dimensions result in steep carrier concentration gradients, which can potentially alter the relative importance of different heat generation mechanisms, including not only the well-established Joule heat[20,21] but also Thomson heat.[22] These two points highlight a critical gap in the current understanding of FinFET heat generation characteristics, which in turn impedes the

application of effective heat generation regulation methods. Given the fundamental relationship between the electrical properties of a device and its heat generation, techniques that regulate these properties offer a promising pathway for modulating heat generation. While doping engineering is a well-established method for tuning electrical characteristics,[23,24] its strategic use to modulate self-heating effects has not been systematically investigated.

In this study, we employed electrothermal simulations based on the drift-diffusion model and phonon Monte Carlo (MC) simulations to investigate the heat generation mechanisms in FinFETs and, on this basis, propose an approach for mitigating self-heating effects through doping engineering, effectively suppressing Thomson heat and reducing the device hotspot temperature. This work aims to provide a potential strategy for thermal management in device applications.

The FinFET structure investigated in this study is illustrated in Fig. 1(a) and is based on the design reported in Ref. 25. The upper silicon portion of the device is divided into the drain, the source (length 45 nm), and the fin (width 8 nm and height 42 nm). Within the fin, two regions are defined: the extension region (length 15 nm) enclosed by the spacer and the channel region (length 20 nm) surrounded by the gate oxide. In addition, the lower portion of the device comprises shallow trench isolation layers (height 40 nm) and the substrate. The drain and source regions are uniformly doped to a high concentration of 2×10^{19} cm^{-3}, whereas the channel region is uniformly doped to a low concentration of 2×10^{16} cm^{-3}. In contrast, the extension region exhibits a Gaussian doping distribution. The electrothermal coupled simulations were developed based on DEVSIM,[26,27] an open-source TCAD platform characterized by high flexibility and extensibility. The heat conduction equation based on Fourier's law and incorporating an effective thermal conductivity was solved to capture the impact of thermal effects on the electrical characteristics. The boundary conditions included a fixed substrate temperature of 300 K, periodic lateral boundaries, and a thermal boundary resistance of 9×10^{-9} m$^2 \cdot$ K/W.[28] The heat generation mechanisms considered comprised Joule heat, recombination heat, and Thomson heat. Electron transport was modeled using the classical drift-diffusion model (DDM).[29] To account for the dependence of carrier mobility on both doping concentration and temperature, the Philips mobility model[30] was adopted. Additionally, surface scattering effects in the silicon thin film were modeled using the Lombardi surface mobility formulation.[31] Furthermore, the Canali model was utilized to incorporate the electric field dependence of mobility.[32] The heat generation profiles obtained from TCAD were further used as inputs to phonon Monte Carlo simulations to evaluate ballistic phonon effects on temperature distribution. This one-way coupling approach is justified because the Joule heat generation profile in the hotspot is primarily governed by the high electric field rather than local lattice temperature. Additionally, Thomson heat is dominated by the steep carrier concentration gradients rather than temperature gradients. The specifics of these simulations and the phonon properties utilized are detailed in Ref. 33. Figure 1(b) shows the output characteristics under these simulation conditions, which demonstrate good agreement with the experimental DC results extracted from Ref. 25.

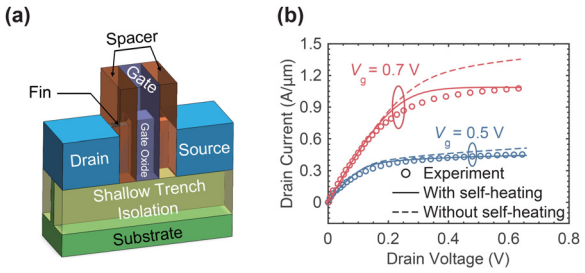

FIG. 1. (a) Schematic of the FinFET. (b) Output characteristics of the FinFET. The lines represent TCAD simulations, and the symbols represent experimental data extracted from Ref. 25.

To analyze the characteristics and underlying mechanisms of different heat generation processes in FinFET devices, a representative CMOS operating bias ($V_g = V_{DD}, V_d = V_{DD}/2$)[19] was selected for simulation, as this condition captures the peak drain current during the switching transient in realistic CMOS circuits ($V_d \approx V_{DD}/2$ and $V_g \approx V_{DD}$),[19] thereby representing the typical heat generation scenario during device operation. Numerical calculations confirm that the contribution of recombination heat is negligible and can thus be excluded from consideration, in agreement with prior studies.[34] Consequently, Joule heat and Thomson heat remain the dominant heat generation mechanisms in transistors. Figure 2 shows the spatial distributions of Joule and Thomson heat in a FinFET device, highlighting their distinct localization characteristics. The spatial distribution of Joule heat primarily depends on the local resistivity within the transistor. The combined effects of doping profiles and field-effect modulation alter the local carrier mobility and carrier concentration; hence, pronounced peaks in resistivity arise in the channel regions near the source and drain terminals. Consequently, as shown in Fig. 2(b), Joule heat exhibits concentrated heat generation near both the drain side and the source side.[35] In contrast, as depicted in Fig. 2(a), Thomson heat exhibits an alternating hot–cold distribution pattern with spatially confined regions of heating and cooling. This alternating polarity is governed by the spatial gradient of thermoelectric power. Specifically, electrons flowing from the source (low thermoelectric power) into the channel (high thermoelectric power) absorb energy, causing negative heat generation (cooling), whereas their injection into the drain releases energy, resulting in positive heat generation. Although the net power of Thomson heat is minimal due to mutual cancelation at different locations, its localized characteristics remain particularly significant, specifically reflected by a peak magnitude comparable to that of Joule heat. Moreover, Thomson heat is confined to extremely narrow regions, predominantly occurring at the drain-extension region, the source-extension region, and the extension-to-channel junctions, where significant carrier concentration gradients exist. This localized heat generation characteristic of Thomson heat may couple with Joule heat to elevate junction temperatures, which in turn can induce pronounced non-Fourier effects.[36]

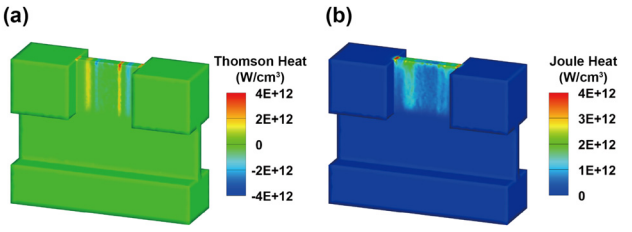

FIG. 2. (a) The Thomson heat and (b) Joule heat distributions of FinFET ($V_g = 0.7$ V, $V_d = 0.35$ V).

To further clarify the impact of Thomson heat on temperature rise, Fig. 3 presents a comparative analysis of heat generation and temperature distributions under two representative bias conditions: the saturation bias ($V_g = V_d = V_{DD}$) and the practical CMOS operating bias ($V_g = V_{DD}, V_d = V_{DD}/2$).[19] Under the former bias condition shown in Fig. 3(a), Joule heat not only constitutes the principal component of the total heat generated but also serves as the primary origin of its non-uniform distribution. However, when the bias is switched to the latter condition, the Joule heat under the practical bias in Fig. 3(c) is markedly reduced and exhibits a more uniform distribution due to its strong dependence on bias.[37] In contrast, Thomson heat shows weak bias dependence and thus remains nearly unchanged across both bias states. This stability arises because Thomson heat is driven by the fixed doping-induced carrier concentration gradient, whereas Joule heat diminishes drastically at lower bias ($V_d = 0.35$ V) owing to the reduction of the pinch-off electric field. As a result, the relative contribution of Joule heat decreases, whereas Thomson heat becomes increasingly significant, and in turn becomes the dominant driver of heat generation non-uniformity, with its peak value accounting for approximately half of the total peak heat generation. The difference in the proportions of Joule heat and Thomson heat under the two bias conditions results in distinct contributions to the overall temperature rise. As illustrated in Figs. 3(b) and 3(d), Thomson heat accounts for only about 5% of the maximum temperature rise under the saturation bias, but its contribution increases to approximately 16%, corresponding to a temperature rise of 9.7 K, under the practical bias condition. These results demonstrate that under practical CMOS operating bias, the thermal impact of Thomson heat becomes considerably more pronounced. Therefore, implementing effective measures to suppress Thomson heat is critical for reducing self-heating and improving the reliability of FinFET devices.

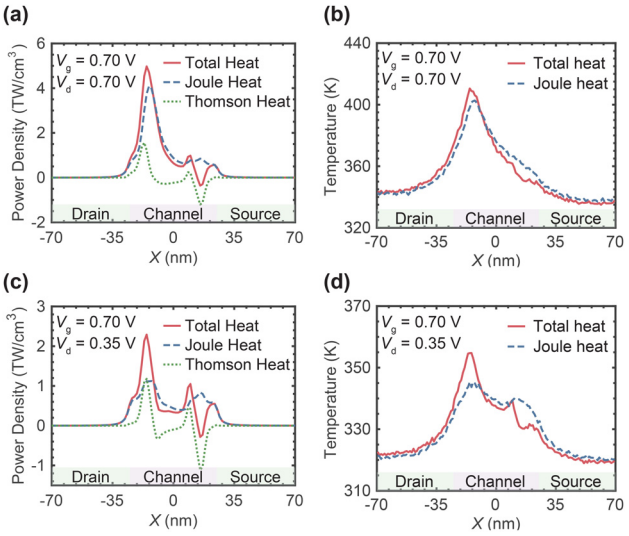

FIG. 3. Heat generation and temperature distributions (obtained from phonon MC simulations) along the channel direction under two representative bias conditions. (a) Heat generation distribution and (b) temperature distribution under $V_g = 0.70$ V, $V_d = 0.70$ V. (c) Heat generation distribution and (d) temperature distribution under $V_g = 0.70$ V, $V_d = 0.35$ V.

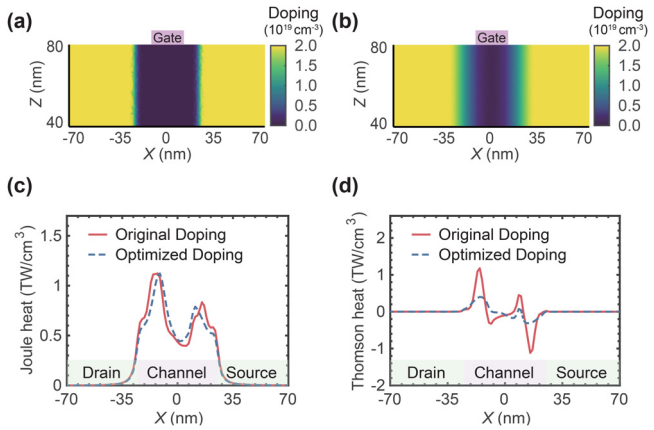

FIG. 4. (a) Original and (b) optimized doping profiles. (c) The Joule heat and (d) Thomson heat distributions under different doping profiles ($V_g = 0.7$ V, $V_d = 0.35$ V).

Since Thomson heat arises primarily from the coupling between internal carrier concentration gradients and temperature gradients,[22] it can therefore be effectively suppressed by tailoring carrier concentration gradients through doping engineering. In doping engineering, it is feasible to adjust the rapid thermal annealing (RTA) conditions to tailor the doping concentration distribution within the extension and channel regions of the FinFET device,[38] which are precisely the regions where Thomson heat is concentrated. Figures 4(a) and 4(b) show the original and optimized doping concentration distributions, respectively. The original doping configuration adopts a relatively steep doping profile, whereas the optimized configuration employs a relatively gradual doping profile. The Joule heat and Thomson heat distribution results after doping profile optimization are presented in Figs. 4(c) and 4(d). While the magnitude and spatial distribution of Joule heat remain nearly unchanged, the Thomson heat shows a substantial reduction, with its peak value decreased by approximately 66%, corresponding to an overall around 33% reduction in peak heat generation. This contrast arises because the Joule heat profile remains stable, as our optimization constrains the drain current to match that of the reference (original doping), ensuring unchanged total resistance. Since Joule heat is dominated by the strong electric field rather than minor resistivity variations in the extension region, it is insensitive to the doping adjustment. This confirms the method's selectivity: it effectively suppresses Thomson heat via the concentration gradient without compromising the electrical performance. Although suppressing the Thomson effect reduces the local cooling near the source, this impact is negligible for thermal reliability. The critical thermal metric is the peak lattice temperature at the drain-side hotspot, which is effectively reduced. Furthermore, by ignoring the endothermic effect of the Thomson heat, the analysis shows that doping optimization reduces its exothermic portion by 48%, an amount equivalent to an 11% reduction in the total exothermic heat generation. These results confirm that adjusting the heat generation distribution through doping engineering is an effective method for thermal management in nanoscale devices.

To provide a clearer illustration of the influence of Thomson heat regulation on the temperature, Figure 5 depicts the temperature distributions obtained before and after doping profile optimization. As

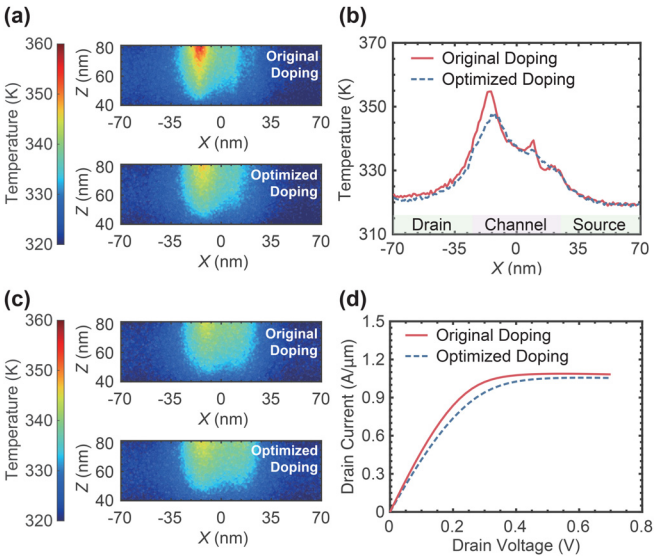

FIG. 5. Thermal and electrical comparison between the original and optimized doping profiles. Temperature distributions obtained from phonon MC simulations ($V_g = 0.7$ V, $V_d = 0.35$ V): (a) considering total heat generation, (b) along the channel at 1 nm depth, and (c) considering solely the Joule heat component. (d) Output characteristics (I_d-V_d) of the device at $V_g = 0.7$ V.

depicted in Fig. 5(a), the area of the hotspot region is noticeably reduced after doping profile optimization, and the local temperature is also significantly decreased. Figure 5(b) further quantitatively illustrates the temperature distribution along the channel direction. The results indicate that, following doping optimization, the maximum temperature rise is reduced by approximately 13% (from 59.2 to 51.6 K), which corresponds to the suppression of most of the temperature rise attributed to Thomson heat. If the meantime-to-failure (MTTF) is used as the reliability metric, where MTTF is proportional to $\exp(E_a/kT_{max})$ with an activation energy $E_a = 1.386$ eV,[39] the doping optimization results in an estimated MTTF increase in approximately 163%. This improvement is highly significant for enhancing device lifetime. To distinguish the contribution of Joule heat, Fig. 5(c) compares the temperature rise considering only the Joule heat component. The results show that the temperature profiles exhibit only a minor variation before and after optimization, with the Joule-induced temperature reduction accounting for only 1.5% of the total temperature rise (approximately 0.9 K). This verifies that the mitigation of the self-heating effect is primarily attributed to the suppression of Thomson heat. Furthermore, Fig. 5(d) presents the output characteristics of the device. The consistency of the $I_d - V_d$ curves confirms that the proposed doping engineering significantly alleviates thermal issues without compromising the electrical performance.

In summary, this work investigates the heat generation mechanisms and influencing factors in FinFETs, and accordingly proposes a method of modulating Thomson heat via doping engineering, thereby mitigating the self-heating effect. It is found that under a saturation bias, heat generation is predominantly caused by the Joule heat. However, under the typical CMOS operating condition, the contribution from Thomson heat becomes significant, emerging as the primary driver of heat generation non-uniformity. In this case, the peak Thomson heat accounts for approximately half of the total peak heat generation and contributes to around 16% of the overall temperature rise. To alleviate the influence of Thomson heat, a strategy for suppressing Thomson heat through doping engineering has been proposed. The device adopting the optimized doping profile characterized by a relatively gradual gradient exhibits a reduction in Thomson heat by approximately 66% and a corresponding decrease in the temperature rise by about 13%(from 59.2 to 51.6 K). This work provides a potential strategy for thermal management in FinFET device applications.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Chenkun Deng: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Writing – original draft (equal). **Zhenglai Tang:** Formal analysis (equal); Methodology (equal); Software (equal); Writing – original draft (equal). **Yang Shen:** Methodology (equal); Software (equal). **Bingyang Cao:** Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

REFERENCES

[1]Q. Zhang, Y. Zhang, Y. Luo, and H. Yin, "New structure transistors for advanced technology node CMOS ICs," Natl. Sci. Rev. **11**, nwae008 (2024).
[2]W. Cao, H. Bu, M. Vinet, M. Cao, S. Takagi, S. Hwang, T. Ghani, and K. Banerjee, "The future transistors," Nature **620**, 501–515 (2023).
[3]U. S. Kumar and V. R. Rao, "A thermal-aware device design considerations for nanoscale SOI and bulk FinFETs," IEEE Trans. Electron Devices **63**, 280–287 (2016).
[4]K. Jenkins and K. Rim, "Measurement of the effect of self-heating in strained-silicon MOSFETs," IEEE Electron Device Lett. **23**, 360–362 (2002).
[5]J. Jeon, H.-S. Jhon, and M. Kang, "Investigation of electrothermal behaviors of 5-nm bulk FinFET," IEEE Trans. Electron Devices **64**, 5284–5287 (2017).
[6]R. J. Warzoha, A. A. Wilson, B. F. Donovan, N. Donmezer, A. Giri, P. E. Hopkins, S. Choi, D. Pahinkar, J. Shi, S. Graham, Z. Tian, and L. Ruppalt, "Applications and impacts of nanoscale thermal transport in electronics packaging," J. Electron. Packag. **143**, 020804 (2021).
[7]S. E. Liu, J. S. Wang, Y. R. Lu, D. S. Huang, C. F. Huang, W. H. Hsieh, J. H. Lee, Y. S. Tsai, J. R. Shih, Y.-H. Lee, and K. Wu, "Self-heating effect in FinFETs and its impact on devices reliability characterization," in *IEEE International Reliability Physics Symposium* (IEEE, 2014), pp. 4A.4.1–4A.4.4.
[8]G. Zhang, S. Dong, Q. Xin, L. Guo, X. Wang, G. Xin, N. Qin, X. Lan, C. Guo, W. Wang, and B. Cao, "Transistor-level thermal management in wide and

ultra-wide bandgap power semiconductor transistors: A review," Int. J. Therm. Sci. **219**, 110200 (2026).
[9]C. Prasad, "A review of self-heating effects in advanced CMOS technologies," IEEE Trans. Electron Devices **66**, 4546–4555 (2019).
[10]C. Chang, K. D. Kook, C. Lin, X. Zhang, Y. Yang, S. Luo, Z. He, T. Li, M. Xu, L. Lau, M. J. H. Emon, R. Rahad, P. Ajayan, J. Lou, S. Kumar, and Y. Zhao, "Mitigation of self-heating in AlGaN/GaN HEMTs using transferred LPCVD-grown h-BN," Appl. Phys. Lett. **127**, 083501 (2025).
[11]J. Sun, X. Li, Y. Sun, and Y. Shi, "Impact of geometry, doping, temperature, and boundary conductivity on thermal characteristics of 14-nm bulk and SOI FinFETs," IEEE Trans. Device Mater. Relib. **20**, 119–127 (2020).
[12]S. Rathore, R. K. Jaisawal, P. N. Kondekar, and N. Bagga, "Demonstration of a nanosheet FET with high thermal conductivity material as buried oxide: Mitigation of self-heating effect," IEEE Trans. Electron Devices **70**, 1970–1976 (2023).
[13]B. Vermeersch, E. Bury, Y. Xiang, P. Schuddinck, K. K. Bhuwalka, G. Hellings, and J. Ryckaert, "Self-heating in iN8-iN2 CMOS logic cells: Thermal impact of architecture (FinFET, nanosheet, forksheet and CFET) and scaling boosters," in *IEEE Symposium on VLSI Technology and Circuits* (IEEE, 2022), pp. 371–372.
[14]P. G. Sverdrup, S. Sinha, M. Asheghi, S. Uma, and K. E. Goodson, "Measurement of ballistic phonon conduction near hotspots in silicon," Appl. Phys. Lett. **78**, 3331–3333 (2001).
[15]L. Zeng, K. C. Collins, Y. Hu, M. N. Luckyanova, A. A. Maznev, S. Huberman, V. Chiloyan, J. Zhou, X. Huang, K. A. Nelson, and G. Chen, "Measuring phonon mean free path distributions by probing quasiballistic phonon transport in grating nanostructures," Sci. Rep. **5**, 17131 (2015).
[16]Z.-L. Tang, Y. Shen, and B.-Y. Cao, "Modulating self-heating effects in GaN HEMTs using slant field plate," IEEE Trans. Electron Devices **72**, 1907–1911 (2025).
[17]X. Guo, V. Verma, P. Gonzalez, S. Mosanu, and M. Stan, "Back to the future: Digital circuit design in the FinFET era," J. Low Power Electron. **13**, 338–355 (2017).
[18]D. Jang, E. Bury, R. Ritzenthaler, M. G. Bardon, T. Chiarella, K. Miyaguchi, P. Raghavan, A. Mocuta, G. Groeseneken, A. Mercha, D. Verkest, and A. Thean, "Self-heating on bulk FinFET from 14 nm down to 7 nm node," in *IEEE International Electron Devices Meeting* (IEEE, 2015), pp. 11.6.1–11.6.4.
[19]K. A. Jenkins and R. L. Franch, "Impact of self-heating on digital SOI and strained-silicon CMOS circuits," in *IEEE International Conference on SOI* (IEEE, 2003), pp. 161–163.
[20]E. Pop, R. W. Dutton, and K. E. Goodson, "Monte Carlo simulation of Joule heating in bulk and strained silicon," Appl. Phys. Lett. **86**, 082101 (2005).
[21]E. Pop, S. Sinha, and K. Goodson, "Heat generation and transport in nanometer-scale transistors," Proc. IEEE **94**, 1587–1601 (2006).
[22]G. Wachutka, "Rigorous thermodynamic treatment of heat generation and conduction in semiconductor device modeling," IEEE Trans. Comput-Aided Des. Integr. Circuits Syst. **9**, 1141–1149 (1990).
[23]C. Han, Y. Liu, K. Liu, H. Yuan, F. Du, Y. Zhou, S. Wang, Z. Wang, X. Tang, Q. Song, and Y. Zhang, "A novel tapered doping tail modulated single junction termination extension for high voltage 4H-SiC devices," IEEE Electron Device Lett. **45**, 1261–1264 (2024).
[24]N. Remesh, N. Mohan, S. Raghavan, R. Muralidharan, and D. N. Nath, "Optimum carbon concentration in GaN-on-Silicon for breakdown enhancement in AlGaN/GaN HEMTs," IEEE Trans. Electron Devices **67**, 2311–2317 (2020).
[25]S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, and K. Zhang, "A 14 nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," in *International Electron Devices Meeting* (IEEE, 2014), pp. 3.7.1–3.7.3.
[26]J. E. Sanchez, "DEVSIM: A TCAD semiconductor device simulator," J. Open Source Software **7**, 3898 (2022).
[27]J. E. Sanchez and Q. Chen, "Element edge based discretization for TCAD device simulation," IEEE Trans. Electron Devices **68**, 5414–5420 (2021).
[28]J. Chen, G. Zhang, and B. Li, "Thermal contact resistance across nanoscale silicon dioxide and silicon interface," J. Appl. Phys. **112**, 064319 (2012).
[29]D. Scharfetter and H. Gummel, "Large-signal analysis of a silicon Read diode oscillator," IEEE Trans. Electron Devices **16**, 64–77 (1969).
[30]D. Klaassen, "A unified mobility model for device simulation-I. Model equations and concentration dependence," Solid-State Electron. **35**, 953–959 (1992).
[31]S. Reggiani, E. Gnani, A. Gnudi, M. Rudan, and G. Baccarani, "Low-field electron mobility model for ultrathin-body SOI and double-gate MOSFETs with extremely small silicon thicknesses," IEEE Trans. Electron Devices **54**, 2204–2212 (2007).
[32]C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," IEEE Trans. Electron Devices **22**, 1045–1047 (1975).
[33]G. Chen, "Thermal conductivity and ballistic-phonon transport in the cross-plane direction of superlattices," Phys. Rev. B **57**, 14958–14973 (1998).
[34]Z.-L. Tang and B.-Y. Cao, "Heat generation mechanisms of self-heating effects in SOI-MOS," IEEE J. Electron Devices Soc. **12**, 350–358 (2024).
[35]Y. Sheng, S. Wang, Y. Hu, J. Xu, Z. Ji, and H. Bao, "Integrating first-principles-based non-Fourier thermal analysis into nanoscale device simulation," IEEE Trans. Electron Devices **71**, 1769–1775 (2024).
[36]Y. Shen, X.-S. Chen, Y.-C. Hua, H.-L. Li, L. Wei, and B.-Y. Cao, "Bias dependence of non-Fourier heat spreading in GaN HEMTs," IEEE Trans. Electron Devices **70**, 409–417 (2023).
[37]Y. Shen and B. Cao, "Two-temperature principle for evaluating electrothermal performance of GaN HEMTs," Appl. Phys. Lett. **124**, 042107 (2024).
[38]A. Veloso, A. De Keersgieter, P. Matagne, N. Horiguchi, and N. Collaert, "Advances on doping strategies for triple-gate finFETs and lateral gate-all-around nanowire FETs and their impact on device performance," Mater. Sci. Semicond. Process. **62**, 2–12 (2017).
[39]K. O. Petrosyants, I. A. Kharitonov, S. V. Lebedev, L. M. Sambursky, S. O. Safonov, and V. G. Stakhin, "Electrical characterization and reliability of submicron SOI CMOS technology in the extended temperature range (to 300 °C)," Microelectron. Reliab. **79**, 416–425 (2017).